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EXAMINER	
YANG, MINCHUL	

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/532,848	BRAUNE ET AL.	
	Examiner	Art Unit	
	Minchul Yang	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/25/08*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-23* is/are pending in the application.

4a) Of the above claim(s) *16 and 21-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-15, 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Election/Restrictions

1. The newly submitted claims 16-23 are directed to inventions which are not related to the inventive concept originally claimed under PCT Rule 13.1 for the following reasons:

I. Claims 1-15, directed toward the species of the method of forming an LED light source, wherein the coating step of the luminescence conversion material is performed without stretching the wafer and with thinning (see, e.g., figures 1f and 2b).

II. Claims 16, directed toward the species of the method of forming an LED light source, wherein the coating step of the luminescence conversion material is performed without stretching the wafer and without thinning (see, e.g., figure 3b).

III. Claims 17-23, directed toward the species of the method of forming an LED light source, the coating step of the luminescence conversion material is performed with stretching the wafer (see, e.g., page 8, last paragraph).

2. The inventions listed are related to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons.

The common technical feature in all groups is the method of forming an LED, comprising steps of preparing the LED chip and thickening the front-side electrical contact. These elements cannot be special technical features under PCT Rule 13.2 because the elements are shown in the prior art (see, e.g., JP Pub. 2002118293: previously made of record of IDS).

Since applicant has received an action on the merits for the originally presented invention (invention I), this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 16 and 21-23 are withdrawn from consideration as being directed to a non-elected invention (claims 1 and 17-19 are generic claims). See 37 CFR 1.142(b) and MPEP § 821.03.

3. Claims 1-4 and 6-23 are pending in the application. Claim 5 is canceled. Claims 15-23 are newly added. Claims 16 and 21-23 are withdrawn from consideration. Claims 1-4, 6-15, 17-20 are examined in this Office action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 6-8, 10-11, 15, 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Tatsunori (JP Pub. 2002118293: previously made of record of IDS).

Tatsunori discloses a method for producing an LED light source, wherein at least a portion of primary radiation emitted by a chip is transformed by luminescence conversion, comprising the steps of (see, e.g., figures 3a-e and related text):

Regarding claim(s) 1: preparing a chip (2) comprising a front-side electrical contact (5) in

the form of an electrical contact surface, the front-side electrical contact being positioned on a principal radiation emitting surface (the top surface of 4) of the LED light source; thickening said front-side electrical contact by applying an electrically conductive material (8) to said electrical contact surface, partially coating said chip with a luminescence conversion material (9) so that at least a portion of the electrically conductive material is not coated with the conversion material (figure 3c: a top surface of the electrically conductive material 8 is not coated with the conversion material 9);

Regarding claim(s) 2-4: wherein said luminescence conversion material comprises a radioparent matrix material and a phosphor (paragraph 0042: the $(Y, Gd)_3(Al, Ga)_5O_{12}$:Ce wavelength conversion material comprises radioparent matrix material Al_2O_3 as a host matrix material and (Y, Gd) as a phosphor); wherein said radioparent matrix material comprises SiO_2 and/or Al_2O_3; wherein said radioparent matrix material comprises an oxide and/or a nitride whose refractive index is between 1.5 and 3.4 (Al_2O_3 has a refractive index between 1.5 and 3.4);

Regarding claim(s) 6, 8: wherein the layer of luminescence conversion material is evened by thinning (see, e.g., figure 3c); wherein the thickness of the layer of luminescence conversion material is adjusted by thinning it (see, e.g., figure 3c);

Regarding claim(s) 7: wherein monitoring of the color coordinates (CIE chromaticity diagram) of the LED light source is subsequently performed (0070);

Regarding claim(s) 10: wherein the chip emitting the primary radiation is disposed in a wafer composite with a multiplicity of additional similar chips (see, e.g., 0012), each of the method steps takes place simultaneously for the chips of the entire wafer composite (see figures 3a-d and related text), the chips are subsequently singulated into LED light sources (figure 3e);

Regarding claim(s) 11: wherein before the chips are coated with luminescence conversion material, troughs (figure 3a: the troughs between the adjacent LED chips) are made along scribe lines between the individual chips, so that during the subsequent coating of the chips with luminescence conversion material said troughs are at least partially filled with luminescence conversion material (figure 3b);

Regarding claim(s) 15: wherein the LED light source is a mixed color LED (at least two colors are generated from the active light emitting layer and the wavelength conversion layer);

Regarding claim(s) 17: preparing a plurality of light emitting chips, each comprising a front-side electrical contact (5) in the form of an electrical contact surface, and disposing the plurality of chips in a wafer composite (1); thickening the front-side electrical contact of each of the chips by applying an electrically conductive material (8) to each electrical contact surface; and coating each of the chips with a luminescence conversion material (9), wherein prior to coating the chips with the luminescence conversion material, the wafer composite is mounted on a carrier material and the chips are at least partially singulated (see figure 3a: note that the wafer must be placed on a carrier material for the partial singulation) so that the chips remain attached to the wafer composite on the carrier material; and wherein during coating of the chips with the luminescence conversion material, lateral surfaces of the at least partially singulated chips are at least partially coated with the luminescence conversion material (figures 3b-3d);

Regarding claim(s) 18: further comprising completing singulation of the plurality of chips from the wafer composite to form a plurality of separated LED light sources (figure 3e);

Regarding claim(s) 19: wherein the electrically conductive material is applied to each member of the plurality of light emitting chips at the same time (0038-0039: the electrically

conductive material is made via plating, and the luminescence conversion material is applied to each member of the plurality of light emitting chips at the same time (figure 3b: the luminescence conversion material is applied at the same time after coating the electrically conductive material and before the thinning process).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tatsunori, as applied to the claims above, in view of Maeda (US Pub. 2002/0028527) and Inoue (US Pub. 2002/0081773).

(a) Regarding claim(s) 9, Tatsunori discloses the features outlined above, but does not expressly teach that the coordinates of the LED device are monitored during thinning.

However, Maeda teaches a method of forming a LED devices wherein the color coordinates of the LED device is adjusted by controlling the thickness of the layers of luminescence conversion (0105 and 0109-0112) using a thinning method. Moreover, it was generally recognized in the art that monitoring optical characteristics of LED devices was performed at a wafer-level before dicing the wafer in order to reduce manufacturing time and cost. For instance, Inoue teaches a method of monitoring optical characteristics of LED devices

at a wafer-level before dicing the wafer (see, e.g., figures 35 and 0295). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to monitor the coordinates of the LED during thinning, as taught by Maeda and Inoue, in the method of Tatsunori in order to reduce manufacturing time and cost.

(b) Regarding claim(s) 14, Tatsunori in view of Inoue teach the following limitation(s), as addressed below regarding claim 13: before the chips are singulated, determining and recording the respective color coordinates and positions of the LED light sources, and monitoring the color coordinates of one of the LED light sources of the region concerned.

Tatsunori in view of Inoue do not expressly teach the following limitation(s): dividing the wafer into regions containing LED light sources that have similar color coordinates, adjusting the regions containing LED light sources that have similar color coordinates to a specific set of color coordinates by regionally selective thinning of the luminescence conversion material in the individual regions. However, Maeda discloses that the color coordinates of the LED device is adjusted by controlling the thickness of the layers of luminescence conversion (0105 and 0109-0112) using a thinning method. Maeda further discloses that each LED device can be selectively thinned in order to adjust its color coordinates (0109-0110 and figures 7a-b). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to perform a selective thinning for a pre-determined region in the wafer of Tatsunori, as taught by Inoue and Maeda, in order to optimize color coordinates such that the color coordinates of the regions are the same or different from each other. The examiner also notes that where the general conditions of a claim are disclosed in prior art, provision for adjustability where needed involves only routine skill in the art.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tatsunori, as applied to the claims above, in view of Kumar (US Pub. 2003/0077878).

(a) Tatsunori discloses the features outlined above, but does not expressly teach the following limitations: wherein before the chips are coated with luminescence conversion material, the entire wafer composite is mounted with the underside on a carrier, the chips are singulated from the wafer composite in such a way that they continue to be held together on said carrier, during the coating of the chips, the lateral sides of the singulated chips are at least partially coated with luminescence conversion material, the chips are subsequently singulated into LED light sources from their composite held together by said carrier and said luminescence conversion material.

However, Kumar teaches a method of singulating a semiconductor chip using a wafer carrier (see, e.g., figure 3d and related text), wherein an entire wafer composite (100) is mounted with the underside on a carrier (300), the chips are singulated from the wafer composite in such a way that they continue to be held together on said carrier (figure 3d), the chips are subsequently singulated from their composite held together by said carrier. Kumar teaches that this method can benefit to avoid the chipping and cracking problems caused by conventional dicing methods (0005-0006). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the Kumar method of singulating chips in the method of Tatsunori in order to avoid the chipping and cracking problems caused by conventional dicing methods. It would also have been obvious to one of ordinary skill in the art at the time of the invention to perform the coating step after the step of singulating the wafer on the wafer carrier in order to simplify the wafer singulating step without need to singulate the coating.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tatsunori, as applied to the claims above, in view of Inoue.

Tatsunori discloses the features previously outlined, but does not expressly teach the following limitation(s): wherein before said chips are singulated into LED light sources their respective color coordinates and positions are determined and recorded, and after singulation the LED light sources are sorted on the basis of their color coordinates.

However, it was a well-recognized practice in the art that monitoring optical characteristics of LED devices was performed at a wafer-level before being singulated in order to reduce manufacturing time and cost. For instance, Inoue teaches a method of monitoring optical characteristics of LED devices at a wafer-level before being singulated (see, e.g., figures 35 and 0295). It was also a well-recognized practice in the art that the step of monitoring optical characteristics of LED devices at a wafer-level included recording positions and color coordinates. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Tatsunori teachings with the Inoue teachings to determine and record color coordinates and positions of the LED devices before being singulated in order to reduce manufacturing time and cost. It would also have been obvious to one of ordinary skill in the art at the time of the invention to sort the singulated LED devices on the basis of their color coordinates, because color of emitting light from the device was critical for applications such as a white light source and a light source for a memory disc.

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tatsunori, as applied to the claims above.

Tatsunori discloses the features previously outlined, but does not expressly disclose the

following limitation(s): wherein the carrier material comprises an adhesive film and/or a stretch film. However, it was well recognized in the art that an adhesive film was used to attach a wafer containing LED chips to a carrier substrate before partial or full singulation. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use an adhesive film to attach the wafer to the carrier substrate in the Tatsunori method because it was well recognized bonding method of a wafer to an underlying carrier substrate for partial or full singulation.

Response to Arguments

11. Applicant's arguments filed on 8/25/08 have been fully considered but are not persuasive for the following reasons.

The applicant's amendment to claim 1 does not overcome the rejections based on Tatsunori. This is because Tatsunori discloses, as addressed above, the front-side electrical contact being positioned on a principal radiation emitting surface (the top surface of 4) of the LED light source; partially coating said chip with a luminescence conversion material (9) so that at least a portion of the electrically conductive material is not coated with the conversion material (figure 3c: a top surface of the electrically conductive material 8 is not coated with the conversion material 9).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minchul Yang whose telephone number is (571) 270-1750. The examiner can normally be reached on Monday through Friday 7:30 AM - 5:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

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MY /M. Y./

Examiner, Art Unit 2891

/Wael M Fahmy/

Supervisory Patent Examiner, Art Unit 2814